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Title of Document: **APPELLANT'S BRIEF ON APPEAL, EXTENSION REQUEST AND APPEAL BRIEF FEE**
Applicant: SAKAMOTO
Serial No.: 09/208105
App. Filed: NOVEMBER 25, 1998
Group Art No.: 2811
Our Ref. No.: 10233.81USW1

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	SAKAMOTO	Examiner:	O. NADAV
Serial No.:	09/208,105	Group Art Unit:	2811
Filed:	NOVEMBER 25, 1998	Docket No.:	10233.81USW1
Title:	SEMICONDUCTOR DEVICE WITH METAL WIRE LAYER MASKING (AS AMENDED)		

CERTIFICATE UNDER 37 CFR 1.6: The undersigned hereby certifies that this correspondence is being sent via facsimile to: The United States Patent & Trademark Office, Commissioner for Patents on July 25, 2005.

By: Lisa Dorn
Name: LISA DORN

APPELLANT'S BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Brief is presented in support of the Appeal filed February 1, 2005, from the final rejection of Claims 9-14 of the above-identified application, as set forth in the Office Action mailed December 16, 2004.

A check for $500.00 to cover the required fee for filing this Brief is enclosed.

I. REAL PARTY OF INTEREST

The Real Party of Interest is ROHM CO., LTD. of 21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto 615-8585, JAPAN.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences for the above-referenced patent application.

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Appellants are unaware of any appeals or interferences that would directly affect or be directly affected by the outcome of the present appeal.

III. STATUS OF CLAIMS

Claims 9-14 are pending and are the subject of this Appeal (Appendix 1, Claims).

IV. STATUS OF AMENDMENTS

No Amendment was filed in response to the final Office Action dated December 16, 2004. Thus, the claims are appealed in the status as of the Amendment dated October 14, 2004, filed in response to the Official Action dated May 4, 2004.

V. SUMMARY OF THE INVENTION

Briefly, Appellants' invention is directed to a semiconductor which has the structure of an electrode being a metal layer which, during manufacture also functions as a mask, so that during the formation of a crystal defect region 11, electron beams from above only primarily penetrate thru an opening 25 in electrode 22. In this way, the formation of defects are limited in a predictable fashion without using external masking.

With reference to specification page 6, line 4, to page 7, line 10, and Figs. 1 and 2, semiconductor 1 is disclosed in the form of a transistor having three electrodes, that is, drain electrode 3, source electrode 22, and gate electrode 17. In substrate 2, n^+ layer 5 and n^- layer 7 are consecutively formed on drain layer 3. A base region 21 is formed in the n^- layer 7. Source regions 23 are formed in the base region 21. An oxidation layer 15 covers the base and source regions. Gate electrode 17 is formed in the oxidation layer 15. Insulating layer 19 covers gate electrode 17, and source electrode 22 formed as a wiring layer made of a light metal connects

with source regions 23, but is otherwise formed on insulating layer 19. Another insulating or passivation layer 29 covers source electrode 22. A silicon oxidation layer 27 is formed on a region 24 located between source regions 23 which are formed within base region 21. Layer 27 functions in combination with insulating layer 19 as an insulator. An opening 25 in source electrode layer 22 is formed above silicon oxidation layer 27. The crystal defect region 11 is formed below opening 25 in the n^- layer 7. Source electrode 22 is made of a light metal, disclosed as aluminum.

VI. ISSUES PRESENTED FOR REVIEW

The only issue from the December 16, 2004, final Office Action presented for review is whether claim 9-12 are non-obvious under 35 USC §103(a) on consideration of Sakamoto (U.S. Patent 5,808,352). Claims 13-14 depend from claims 9-12.

VII. GROUPING OF CLAIMS

For purposes of the present appeal only, claims 9-14 are considered to stand or fall together.

VIII. ARGUMENT

Claims 9-12 are non-obvious in view of Sakamoto.

Sakamoto discloses a semiconductor having a collector electrode 22 with n^+ and n^- type layers thereon. A p-type base 12 is formed in the n^- type layer 11 with an n^+ emitter 13 formed in the base. A protective film 16 covers the n^- type layer 11 and portions of base 12 and emitter 13. A silicon nitride film 17 is provided on protective film 16 in an area which is external to the perimeter of base 12. Base electrode 18 and emitter electrode 19 are made of aluminum and are

aluminum and are provided on the silicon nitride film 17 while also making contact with base 12 and emitter 13, respectively. With respect to the purpose of the silicon nitride layer 17, Sakamoto states as follows:

> To fabricate the transistor of example 1, the silicon nitride film 17 is provided before the semi-conductor layer 11 is given overall exposure to an electron beam to create crystal defects 21 in that layer 11. Many crystal defects 21 are formed under the base region 12, but only few crystal defects 21 are created in the field region which surrounds the base region 12 (the number of crosses in FIG. 1 is a relative measure of the number of crystal defects present). Thus, the silicon nitride film 17 which restrains the exposure to an electron beam is provided in the surface of the semiconductor layer 11 to cover the field region before actual exposure to electron beams. Because of this configuration, an electron beam is admitted unattenutated into the semiconductor layer 11 in the base region 12 which has no overlying silicon nitride film, thereby creating many crystal defects 21. On the other hand, the field region which is provided with the silicon nitride film 17 effectively restrains the penetration of electron beam so that only a limited amount of the electron beam will reach the semiconductor layer 11 to create a correspondingly smaller number of crystal defects 21.

Sakamoto, column 5, line 64 to column 6, line 16.

Two different electrodes, namely, base electrode 18 and emitter electrode 19 are formed on the silicon nitride film 17. Each of the electrodes extends beyond the silicon nitride 17 to make contact with base 12 or emitter 15.

In the rejection of claims 9-12, the Examiner states in part:

> ... and a light medal wiring layer 18, 19, comprising aluminum located over the substrate accept at openings above the regions irradiated and connected to each of the impurity regions, wherein radiating rays passing to the regions irradiated through the openings and generating crystal defects under the openings so that a smaller amount of radiating rays are irradiated elsewhere in the substrate compared with the regions under the openings. Sakamoto does not state that the metal wiring layer is located over the entire substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the metal wiring layer over the entire substrate...

Final action dated December 16, 2004, page 2, line 19 to page 3, line 6.

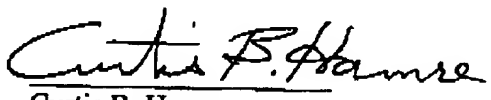
It would not be obvious to form the metal wiring layer over the entire substrate. Sakamoto teaches the use of the silicon nitride film to be installed and used as a mask when an electron beam is directed toward base 12. The silicon nitride film might be located over the entire substrate, except over base 12. The silicon nitride film is not a "metal wiring layer" as required by claim 9; it is a mask. Rather, Sakamoto has two electrodes 18 and 19 which are metal wiring items. Neither one of them could cover the entire substrate without subsuming the other and completely changing the structure of Sakamoto. The Examiner would like the silicon nitride film 17 of Sakamoto to be one of the electrodes 18 or 19 of Sakamoto. It cannot be, and it is not obvious from a consideration of the silicon nitrate film 17 of Sakamoto to obtain structure claimed in claim 9, particularly:

> a metal wiring layer located over the entire substrate except at openings above the regions irradiated .... the metal wiring layer being connected to each of the impurity regions...

The silicon nitride film of Sakamoto is not an element which is connectable to each of the impurity regions. The electrodes of Sakamoto cannot be located over the entire substrate except at openings above the regions irradiated since one of them would then subsume the other and change the structure of Sakamoto. Claim 9 and the claims which depend from it are not obvious on consideration of Sakamoto.

Respectfully Submitted,

Dated: July 25, 2005



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APPENDIX 1

THE CLAIMS ON APPEAL (as finally amended)

1-8. (Cancelled)

9. (Previously presented) A semiconductor device comprising:

a substrate having a regions irradiated with radiating rays,

crystal defects within the regions irradiated,

impurity regions formed in the substrate, and

a metal wiring layer located over the entire substrate except at openings above the regions irradiated, wherein radiating rays passing to the regions irradiated through the openings generate the crystal defects under the openings and so that a smaller amount of radiating rays are irradiated elsewhere in said substrate as compared with said regions under the openings, the metal wiring layer being connected to each of the impurity regions, the metal wiring layer being made of a light metal.

10. (Previously presented) The semiconductor device in accordance with Claim 9, wherein the metal wiring layer is formed in a thickness so the smaller amount of radiating rays are irradiated elsewhere in said substrate except the regions under the openings.

11. (Previously presented) The semiconductor device in accordance with Claim 10, wherein an insulating layer is formed above the regions irradiated, the openings being on the insulating layer.

12. (Previously Presented) The semiconductor device in accordance with Claim 11, wherein the metal wiring layer covers a part of the insulating layer.

13. (Previously presented) The semiconductor device in accordance with Claim 12, wherein the semiconductor device is an insulated gate bipolar transistor, wherein one of the impurity regions is a source region, and wherein one of the regions irradiated is a positive-negative junction where a parasitic diode is generated.

14. (Previously presented) The semiconductor device in accordance with Claim 12, wherein the semiconductor device is a metal oxide semiconductor field effect transistor, wherein one of the impurity regions is a source region, and wherein one of the regions irradiated is a positive-negative junction region where a parasitic diode is generated.

APPENDIX 2

OFFICE ACTIONS AND AMENDMENTS/RESPONSES (See File History)

A. Final Office Action – mailed December 16, 2005.

B. Amendment – mailed October 14, 2004.

C. Office Action – mailed May 4, 2004.

D. RCE – mailed April 22, 2004 (Amendment under Rule 116 entered)

E. Advisory Action – mailed April 14, 2004.

F. Amendment under Rule 116 (Not entered) – mailed March 16, 2004.

G. Final Office Action – mailed October 27, 2003.

H. Amendment – mailed August 5, 2003.

I. Office Action – mailed April 25, 2003.

J. RCE – mailed March 6, 2003 (PTO did not received Amendment under Rule 116 mailed November 6, 2002)

K. Amendment under Rule 116 – mailed November 6, 2002.

L. Final Office Action – mailed September 6, 2002.

M. Amendment – mailed June 24, 2002.

N. Office Action – mailed February 22, 2002.

O. RCE and Amendment under Rule 116 – mailed October 19, 2001.

P. Final Office Action – mailed May 15, 2001.

Q. Amendment – mailed February 28, 2001.

R. Office Action – mailed September 29, 2000.

APPENDIX 3

REFERENCES RELIED UPON BY THE EXAMINER

A. Sakamoto (US Patent 5,808,352)